ABSTRACT OF THE DISCLOSURE

[00062] A semiconductor memory device and a method for manufacturing the same are provided. The semiconductor memory device includes an oxide layer for isolating individual devices which define device areas so that a cell area and a peripheral circuit area are separated from each other on a semiconductor substrate, a plurality of MOS transistors, which are comprised of source areas, drain areas, and gates that are formed in the cell area and the peripheral circuit area, a bit line, which is formed on the plurality of MOS transistors and is electrically connected to the MOS transistor, a stack-shaped capacitor, which is comprised of a first electrode, a dielectric layer, and a second electrode between which the MOS transistors and the bit line in the cell area is interposed, a guard-ring pattern, which are interposed between the cell area and the peripheral circuit area, surrounds the cell area and is apart from the peripheral circuit area, and a contact fill for plate electrode, which is formed in the guard-ring pattern and is in contact with the second electrode that is formed on the internal sidewall and the bottom of the guard-ring pattern. The guard-ring pattern is formed in a boundary between the cell area and the peripheral circuit area while surrounding the cell area, and thereby step caused by manufacture of the stack-shaped capacitor are removed during a manufacturing process, and the contact fill for plate electrode is formed in the guard-ring pattern, and thereby the ground resistance of the capacitor is reduced, and the electrical characteristics of the memory device are improved.